Low-Power Traceback MAP Decoding for Double-Binary Convolutional Turbo Decoder

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***Abstract*—Convolutional turbo decoding requires large data access and consumes large memories. To reduce the size of the metrics memory, the traceback MAP decoding is introduced for double-binary convolutional turbo codes without losing the correction performance. The traceback technique reduces the metrics memory size with no other checkers which prolong the decoding latency. Two proposed traceback structures have a tradeoff between the power and operating frequency. The traceback structures can achieve around 20% power reduction of the metrics memory and around 7% power reduction of the decoders for WiMAX standard.**

I. INTRODUCTION

Binary convolutional turbo code (CTC) proposed in 1993 [1] has been proved that it can get a high coding gain near the Shannon capacity limit. In 1999, the non-binary CTC [2] was introduced to have superior coding gain. In recent years, the double-binary CTC was adopted in the advanced wireless communication standards, such as DVB-RCS [3], and WiMAX [4].

The reduction of the CTC in bit error rates is achieved at the expense of intensive computations involved in the iterative turbo decoding steps. The iterative turbo decoding is composed of soft-input soft-output (SISO) decoding algorithms. A powerful SISO algorithm is the maximum *a posteriori* probability algorithm (MAP). Because of additive forms of the log-MAP (L-MAP) and Max-log-MAP (ML-MAP), they have been widely used in MAP algorithms. An enhanced Max-log-MAP (EML-MAP) has been proposed to have much better coding gain than the ML-MAP [5]. Without massive mathematical approximations, the L-MAP however has the significant correction performance than the (E)ML-MAP.

The memory organization of the metrics in MAP algorithms is critical. For binary CTC decoders, some previous works have been proposed to reduce power consumptions based on decreasing size or accesses of the memory [6]-[7]. The reverse calculations with a flag memory and reversion checkers are proposed in [7], [8]. The reversion checkers prolong the decoding critical path or cycles. Besides, the reverse calculation in [8] only works in (E)ML-MAP. Our previous work [6] was proposed to trace the metrics back. The traceback calculation works with low logic overhead in the L-MAP and (E)ML-MAP. Fig. 1 illustrates the decoding paths of the conventional and traceback computation. In the conventional path, the state metrics computed by natural recursion processor (NRP) in the natural order are stored in the metrics memory (MM). Then, the state metrics are read out to compute *log-likelihood ratio* (LLR) in the reverse order. In the traceback path, the difference metrics are stored in the MM. Then, the state metrics are traced back in the reverse order with the stored difference metrics. Instead of storing all state metrics, the size of MM can be reduced by access the difference metrics.

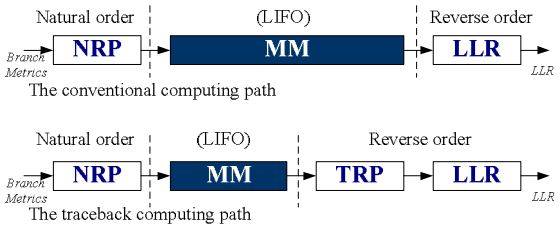

Figure 1. Decoding path for metrics access.

The double-binary CTC complicates the computational complexity of SISO decoding due to the radix-4 trellis. The reverse calculation requires more complicated reversion checkers because the trellis becomes from radix-2 to radix-4. In the literatures, there are seldom works discussing the memory organization of the double-binary CTC decoders. In this paper, the traceback technique for double-binary CTC is introduced. Two pairs of the traceback technique are demonstrated to reduce power consumptions of the MM.

II. FUNDAMENTALS OF MAP ALGORITHMS

In double-binary CTC decoding, MAP algorithms decides binary information bits $u_k = (x^1_k, x^2_k)$ at time k on the values of the *a posteriori* information. Initially, the arithmetic operations of the ML-MAP are described as follows. The branch metrics are

$$\gamma_k^{(z)}(S_{k-1}, S_k) = \Lambda_{apr,k}^{(z)}(u_k = z) + 2\sum_{i=1}^{4} y_k^i x_k^i \qquad (1)$$

This work is supported by the SoC Technology Center (STC) at Industrial Technology Research Institute (ITRI), under the WiMAX FEC project.

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where $\Lambda^{(z)}_{apr,k}$ is *a priori* information, and $z \in \{00, 01, 10, 11\}$. x^i_k denotes the transmitted codewords, and y^i_k denotes received codewords. The state metrics are

$$\alpha_k(S_k) = \underset{S_{k-1}}{MAX}(\gamma^{(z)}_k(S_{k-1}, S_k) + \alpha_{k-1}(S_{k-1})), \tag{2}$$

$$\beta_k(S_k) = \underset{S_{k+1}}{MAX}(\gamma^{(z)}_{k+1}(S_k, S_{k+1}) + \beta_{k+1}(S_{k+1})), \tag{3}$$

where α_k is the forward recursion state metrics, β_k is the backward recursion state metrics.

The *a posteriori* information $\Lambda^{(z)}_{apo,k}$ is defined as

$$\begin{aligned}\Lambda^{(z)}_{apo,k}(u_k) = &\underset{S_k, S_{k+1}, u_k=z}{MAX}(\alpha_k(S_k) + \gamma^{(z)}_{k+1}(S_k, S_{k+1}) + \beta_{k+1}(S_{k+1})) \\ &- \underset{S_k, S_{k+1}, u_k=00}{MAX}(\alpha_k(S_k) + \gamma^{(00)}_{k+1}(S_k, S_{k+1}) + \beta_{k+1}(S_{k+1})).\end{aligned} \tag{4}$$

Decisions $u_k = z$ are based on

$$z = \arg_z(MAX(\Lambda^{(00)}_{apo,k}(u_k), \Lambda^{(01)}_{apo,k}(u_k), \Lambda^{(10)}_{apo,k}(u_k), \Lambda^{(11)}_{apo,k}(u_k))). \tag{5}$$

During the operations of the turbo decoding, one value has to be iteratively interleaved and fed back to the ML-MAP algorithm as *a priori information*. This value called *extrinsic information* $\Lambda^{(z)}_{ex,k}$ is defined as

$$\Lambda^{(z)}_{ex,k}(u_k) = \Lambda^{(z)}_{apo,k}(u_k) - \Lambda^{(z)}_{apr,k}(u_k) - \Lambda^{(z)}_{in,k}(u_k). \tag{6}$$

The intrinsic information $\Lambda^{(z)}_{in,k}$ is defined as

$$\begin{cases}\Lambda^{(00)}_{in,k}(u_k) = 00, \\ \Lambda^{(01)}_{in,k}(u_k) = 4y^2_k, \\ \Lambda^{(10)}_{in,k}(u_k) = 4y^1_k, \\ \Lambda^{(11)}_{in,k}(u_k) = 4(y^1_k + y^2_k).\end{cases} \tag{7}$$

Note that the values of the $\Lambda^{(00)}_{apr,k}$, $\Lambda^{(00)}_{apo,k}$, $\Lambda^{(00)}_{ex,k}$, and $\Lambda^{(00)}_{in,k}$, are always zeros.

The difference between EML-MAP and ML-MAP is that $\Lambda^{(z)}_{ex,k}$ (7) multiplies an scaling factor ($0 < \theta < 1$) in EML-MAP. The differences between L-MAP and ML-MAP are that $\Lambda^{(z)}_{in,k}$ (8) multiplies the channel value and replacing *MAX* operations in (2)-(4) are replaced by *MAX** in L-MAP. The *MAX** is defined as

$$MAX^*(x, y) = \ln(e^x + e^y) = MAX(x, y) + \ln(1 + e^{-|x-y|}). \tag{8}$$

A look-up table (LUT) can implement the corrective term $ln(1+e^{-|x-y|})$.

III. Traceback Computation for Radix-4 Trellis

Fig. 2(a) shows an example of the 8-state radix-4 trellis of the natural recursion for double-binary CTC. The t denotes the time index and the k denotes the symbol index. The natural recursion can be the forward recursion or the backward recursion. In the natural recursion, the 8 states metrics are recursively computed by the NRP. The NRP is composed of 8 add-compare-select (ACS) units. In general, the forward (2) and backward (3) recursion states metrics are computed in chronologically reverse order. Both forward and backward recursion state metrics are required for computation of the $\Lambda^{(z)}_{apo,k}$ (4), so it is necessary that a large size of MM stores the forward (or backward) recursion state metrics to compute the $\Lambda^{(z)}_{apo,k}$ until the backward (or forward) recursion state metrics are generated.

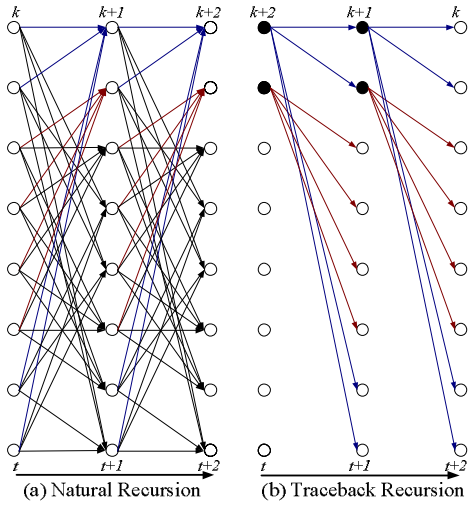

Figure 2. The trellis evolutions of the (a) natural recursion, and (b) traceback recursion.

In this paper, the traceback technique is extended from the radix-2 to radix-4 trellis. Fig. 2(b) shows the traceback recursion of the radix-4 trellis for double-binary CTC. Instead of storing the all state metrics, the difference metrics computed by the ACS units are stored in the MM when the natural recursion generates the state metrics. The traceback recursion regenerates the state metrics with the stored difference metrics by the traceback units. The TRP composed of only 2 traceback units (black states in Fig. 2(b)) recomputes the 8 state metrics. Thus, the traceback technique can reduce the MM size with low logic overhead, and require no flag memory and no reversion checker which prolongs the decoding latency. The traceback calculation works in the L-MAP, and (E)ML-MAP. Note that the proposed traceback technique can be simply applied to the radix-4 trellis of binary CTC with some modifications.

IV. ACS Units and Traceback Units

For a radix-4 trellis of double-binary CTC, there are 4 state inputs to compute a state output. We demonstrate 2 types of the ACS unit and corresponding traceback unit for

the L-MAP and radix-4 trellis. In the L-MAP, a LUT implements the corrective term $ln(1+e^{-x})$. Note that all structures described in this section perform (E)ML-MAP if the LUT is not used. Fig. 3 shows an example of the radix-2x2 ACS unit. The radix-2x2 ACS unit consists of 3 radix-2 ACS units and a LUT. In the traceback technique, 3 difference metrics (*Diff_0, Diff_1 and Diff_2*) of the radix-2x2 ACS unit are stored in the MM. Fig. 4 shows the corresponding traceback unit of the radix-2x2 ACS unit. With 3 difference metrics stored in the MM, the state metrics can be recomputed by the traceback unit. Because 2 current states can trace 8 next states back, there are totally 6 difference metrics stored in the MM. The storage of the MM is reduced from 8 state metrics to 6 difference metrics.

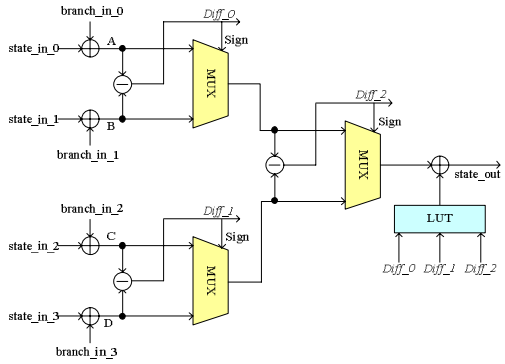

Figure 3. The radix-2x2 ACS unit

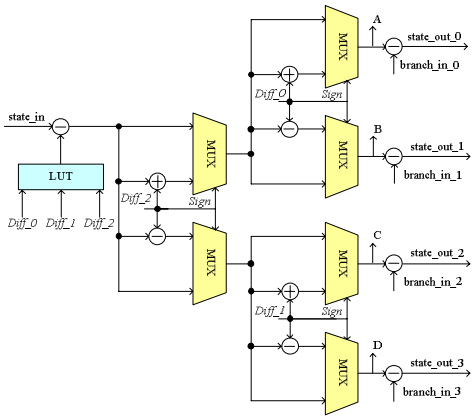

Figure 4. The corresponding traceback unit of the radix-2x2 ACS unit.

The second type is the radix-4 ACS unit which has shorter critical path but larger complexity than the radix-2x2 ACS unit. Fig. 5 shows an example of the radix-4 ACS unit. The radix-4 ACS unit has a comparator to select maximal metrics quickly. Unlike the radix-2x2 ACS unit, 3 difference metrics (*Diff_0, Diff_1* and *Diff_2*) and 2 selective bits (S0 and S1) of the radix-4 ACS unit are stored in the MM. Fig. 6 shows the corresponding traceback unit of the radix-4 ACS unit. Compared with the traceback unit of the radix-2x2 ACS unit, the traceback unit of the radix-4 ACS unit has less complexity. The storage of the MM is reduced from 8 state metrics to 6 difference metrics and 4 extra bits. Note that the terms of state metrics plus branch metrics in the output end of the traceback units (A, B, C, D in Fig. 4 and Fig. 6) can be the input values of the LLR unit to compute $\Lambda^{(z)}_{apo,k}$ (4). This approach reduces 8 adders in LLR unit.

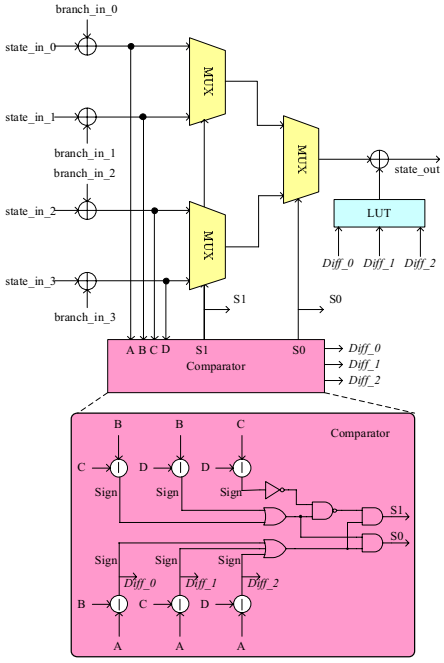

Figure 5. The radix-4 ACS unit.

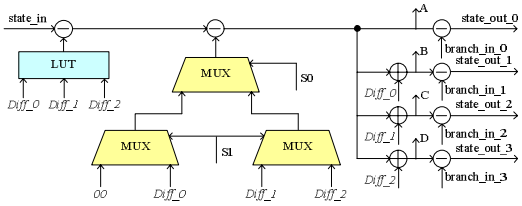

Figure 6. The corresponding traceback unit of the radix-4 ACS unit.

V. Experimental Results

A fast and accurate hardware evaluation and power estimation approach is obtained by using Verilog HDL codes synthesized with the standard cell library of TSMC 0.13-μm CMOS Process. Table I shows evaluation parameters under the specification of WiMAX standard. To support the high throughputs of the WiMAX CTC, the traceback structures are estimated in the parallel-window (PW) [9] EML-MAP decoding.

Table II shows the results of silicon area and power consumptions of the different structures. The radix-4 ACS unit and its corresponding traceback unit are represented as radix-4 pair, and the radix-2x2 ACS unit and its corresponding traceback unit are represented as radix-2x2 pair. The area results are reported by Synopsis Design Vision. The power consumptions on 2-dB SNR noisy data are estimated by Synopsis PrimePower at 100 MHz operating

frequency. 8 ACS units (as a NRP) and 2 traceback units (as a TRP) are grouped as an example of the traceback structure. The results show that the radix-2x2 pair has less hardware cost and power consumptions. The radix-4 pair has shorter and more balanced critical path. It is a tradeoff between the power consumptions and maximal operating frequency.

TABLE I. SEPCIFICATION OF DECODING FOR WIMAX CTC

Decoding algorithm	Parallel-window (PW) EML-MAP
Block size	240
Number of iterations	4 (fixed)
Number of parallel window	10
Size of parallel window	24
Quantization (Total bits, Fractional bits)	y^i_k : (5,3) $\gamma^{(z)}_k$, $\Lambda^{(z)}_{ex,k}$: (9,3) α_k, β_k : (10,3) $\Lambda^{(z)}_{apo,k}$: (11, 3)

TABLE II. THE EXPERIMENTAL RESULT OF THE DIFFERENT STRUCTURES. (TSMC 0.13µm Process, @100MHz)

Pair	Units	Critical Path (ns)	Area (μm^2)	Power (mW) @100MHz
Radix-2x2	8 ACS	9.35	18540.70	0.65
	2 Traceback	6.02	8276.52	0.08
Radix-4	8 ACS	5.77	22157.86	0.75
	2 Traceback	5.51	5822.08	0.05

In Table III, the single-port RAM in TSMC 0.13µm Process is generated for the evaluations of the three different MM. Note that 8 state metrics have to be stored in the MM despite the conventional organization composed of the radix-2x2 or radix-4 units. Thus, the traceback organization of the radix-2x2 pair achieves 24.9% area reduction of the RAM (0.011 mm^2) with 18.8% area overhead of the traceback units (0.008 mm^2), and it also achieves 25% power reduction of the MM (0.55 mW) with 3.6% power overhead of the traceback units (0.08 mW). The traceback organization of the radix-4 pair achieves 19.6% area reduction of the MM (0.009 mm^2) with 13.2% area overhead of the traceback units (0.006 mm^2), and it also achieves 19.5% power reduction of the RAM (0.43 mW) with 2.3% power overhead of the traceback units (0.05 mW).

Table IV shows the area and power comparisons of the 10-SISO PW decoders which meet the specification in Table I. The decoders operate at clock frequency of 100 MHz and achieve throughput rate of 115.4Mbps. Because the double-binary CTC complicates the computational complexity of decoders (*e.g.* LLR units and branch metrics units) the silicon area is not reduced significantly. However, the power consumptions of the 10-SISO PW decoders are noticeably decreased in the traceback organizations.

In addition, an implementation of a 12-mode WiMAX-compliant CTC decoder with the radix-2x2 traceback pair will be detailedly presented in [10].

TABLE III. THE SINGLE-PORT RAM COMPARISON OF THE DIFFERENT ORGANIZATIONS. (TSMC 0.13µm Process, @100MHz)

Organization	MM Size (Words x Bits)	Memory Area (μm^2)	Power (mW) @100MHz
Conventional	12x80	44061.11	2.20
Traceback (Radix-2x2)	12x60	33075.37	1.65
Traceback (Radix-4)	12x64	35417.95	1.77

TABLE IV. THE AREA AND POWER COMPARISONS OF THE 10-SISO PW DECODERS FOR WIMAX CTC. (TSMC 0.13µm Process, @100MHz)

Organization	Area (mm^2)	Power (mW) @100MHz
Conventional (Radix-2x2)	2.56 (97.34%)	117.53 (94.75%)
Traceback (Radix-2x2)	2.51 (95.43%)	108.31 (87.31%)
Conventional (Radix-4)	2.63 (100%)	124.04 (100%)
Traceback (Radix-4)	2.57 (97.72%)	116.44 (93.87%)

VI. CONCLUSIONS

To reduce the MM size, the traceback MAP decoding for double-binary CTC is proposed in this paper. Two pairs of the ACS unit and its corresponding traceback unit are introduced for radix-4 trellis. The radix-2x2 pair has low hardware cost and the radix-4 pair has short critical path. The experimental results in TSMC 0.13-µm CMOS Process at 100MHz operating frequency show that the traceback organization of the radix-2x2 pair achieves 25% power reduction of the MM. The traceback organization of the radix-4 pair achieves 19.5% power reduction. The proposed traceback structures can achieve around 7% power reduction of the 10-SISO PW decoders for WiMAX CTC.

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