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Development of High-Current Solid-State Power Controllers for Aircraft High-Voltage DC Network Applications

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ABSTRACT Solid-state power controllers (SSPCs) have been received increasing attention as they can configure the electrical system and protect the system by fast tripping mechanism at the same time. Although the high-voltage direct current (HVDC) electrical system can bring sustainable savings on the cables' weight and losses, the protection can be considerably challenging. SSPCs have been successfully utilized for 28V DC aircraft onboard network. However, high-voltage ones are impeded by the vast over-voltage and the excessive losses generated from SSPC switching. This paper tries to fill this gap and presents the development of high-power SSPCs for a ±270VDC network of a future turboprop aircraft. Comprehensive designs of proper over-voltage suppression along with SSPC thermal management are presented in this paper. Besides, a comparative study on the SSPC device is carried out. Two prototypes, including a single MOSFET module and paralleling several discrete MOSFET devices, are built and then tested in the experiment. It has been validated that the proposed voltage clamping design can not only effectively suppress the over-voltage, but also limit the SSPC temperature increase during switching for both candidates. After comparing the conduction losses, maximum junction temperature, power density, weight and volume, the single device solution is recommended as a preferable SSPC option for future aircraft.

INDEX TERMS More-electric Aircraft, solid state power controller, thermal analysis, voltage clamping.

I. INTRODUCTION

The fossil fuel-driven aerospace industry contributes about 3% of the global CO_2 emission [1]. Recently, the electrification of aircraft has been extensively researched to reduce carbon footprints for future aircraft. The conventional mechanical, hydraulic, pneumatic systems on-board aircraft are gradually displaced by their electrical counterparts. The electrification of the aircraft will potentially reduce the overall CO_2 and NO_x emissions as well as the noise of aircraft. In addition, more-electric aircraft (MEA) exhibits reduced vibrations, increased maintainability and survivability over the existing architecture [1], [2].

The constant frequency-based electrical system of the aircraft (115 V/400 Hz) has been employed widely in conventional aircraft (A320 and B737 for example). This architecture consists of a bulky constant speed drive which changes a variables speed of aircraft engine to a constant speed and driving electrical generator shaft. A bipolar ±270V DC (HVDC) system has been proposed recently for civil aircraft application recently, which can potentially reduce the weight of the overall aircraft cables [1]–[3]. Within this system, electrical power from generators is converted into ±270 V through power electronic devices and fed into electrical power distribution centres (EDPCs). These EPDCs supply power to several secondary power distribution units (SPDUs). The SPDUs consists of various loads rated for 270 V and 28 V. The overall schematic of a ±270 V electrical system architecture for future aircraft is shown in Fig. 1.

The protection of power cables between are EPDCs and generator power converters are carried out employing the high current/high voltage circuit breakers. The conventional electromechanical circuit breakers (ECBs) have inherent

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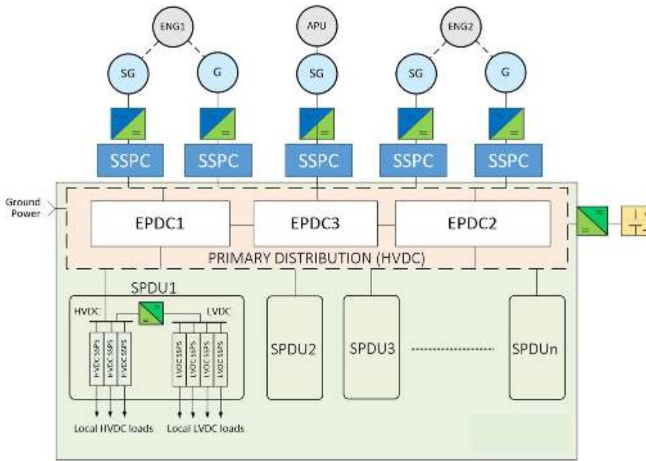

FIGURE 1: A simplified electrical power system of a more electric aircraft with high current SSPCs [1].

arching problem and reliability issue if used in DC application [4]. This is due to the absence of voltage zero-crossing in the DC network. Therefore, solid state power controllers (SSPCs) are extensively researched for MEA applications [5]–[8]. The SSPCs consist of semiconductor switches (one or many in parallel) that suffers significantly higher conduction loss than that of the ECBs. On the other hand, HCB (hybrid circuit breaker) poses the benefits of both ECB and SSPC. However, the design and operation of the HCB are complicated and expensive as compared with the other two circuit breakers such to achieve the same level of switching speeds [5]–[8].

Various topologies of semiconductor-based SSPCs and their technological advancements are presented in [5]–[15]. The design of SSPC employing SiC JFETs is explained in [5]. The SSPC rated for 600 V/60 A is experimentally validated in the laboratory environment. The thyristor-based hybrid circuit breakers for very high voltage application (15 kV) have been demonstrated in [7], [8]. In [10], the experimental demonstration of the SSPC based on (MOS)-controlled thyristor (MCT) have been published. The over-voltage protection for the SSPC is one of the main design challenges, which have been discussed in [13], [14], [16], [17]. However, to the best of our knowledge, the comparative design of high current SSPCs with different semiconductor devices has not been reported in the literature.

The SSPC is a 'normally on' semiconductor switch/switches carrying continuous current throughout its life. The breaking current of SSPC can be four to ten times higher than the nominal current [5], [6]. Therefore, the semiconductor devices employed in an SSPC should withstand both nominal and over-current conditions. The high current SSPC can be realised in two ways, either by using a single high current MOSFET module or using parallel loops of discrete MOSFETs. The use of high current module reduces the device number. However, the conduction loss of SSPC would be dissipated across the single module. On the other hand, the multiple loops of smaller components (TO-247 package for example) increase the component number and switching them synchronously would be a challenging task. Detailed studies of SSPCs with two different design approaches have not been carried out in the past and therefore is the focus of this paper. The purpose of this paper is to provide the comprehensive analysis and overcome two main design challenges for the development of the high-voltage high-current SSPCs, which are: 1) The thermal stability during nominal condition (always on) and over-load conditions (during over-current trip); 2) Over-voltage protection during over-current trip.

This paper presents a comprehensive design of 100 A SSPC rated at ±270 V for civil tilt rotor-craft (CTR) applications. First, the SSPC is designed employing high current SiC MOSFET modules with considerably high cost. The same rating SSPCs can also be built using multiple channel SiC discrete MOSFETs (TO-247 package). The detailed thermal analysis and protection mechanisms of these two types of SSPCs are also included in this paper.

The rest of the paper is organized in the following manner. Section II outlines the specifications and device selection of the DC SSPC for next-generation CTR. The thermal evaluation of both SSPCs is presented in Section III. The protection mechanism for the SSPCs is explained in Section IV. The experimental results and comparative evaluation for both the design approaches are included in Section V and VII, respectively.

II. SPECIFICATION AND DESIGN CONSIDERATION OF THE DC SSPC

The SSPCs are designed to operate at a nominal current of 100 A in an ambient temperature of 85 $^{\circ}C$. From the design specification of the DC SSPC shown below, the approximate I^2t tripping curve is generated and presented in Fig. 2. This SSPC tripping curve considers the upstream power generation capabilities of the electrical generator and its protection mechanism.

- Nominal voltage rating: ± 270 V
- Nominal current rating: 100 A
- Pulse current rating: 100*4 A (400 A for 1 ms), 100*2 A (200 A for 10 ms), 100*1.5 A (150 A for 5 s), 100*1.25 A (125 A for 120 s)

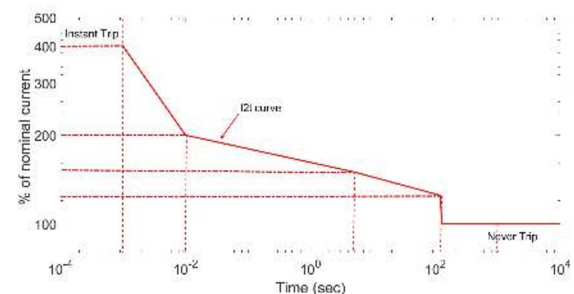

FIGURE 2: The approximated I^2t curve of the proposed DC SSPC.

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For the thermal simulation studies, assumed line impedances are mentioned below:

- DC transmission line impedance: R_{DC}= 0.1 $m\Omega$, L_{DC}= 15 μH

For the design of SSPCs, trade-off studies have been carried out within the project. As a trade-off study output, a CREE module (CAS325M12HM2) with low on-state resistance is chosen for single device configuration and another CREE module C2M0025120D (TO-247 package) is selected for multiple parallel devices configuration. The ratings of the selected semiconductor devices are presented in Table 1.

TABLE 1: The semiconductor devices selected for the SSPC design

No	Parameters	CAS325M12HM2	C2M0025120D
1	Supplier	CREE	CREE
2	$R_{ds(on)}$	4 $m\Omega$	25 $m\Omega$
3	V_{ds} in V	1200	1200
4	T_{jmax} ($^{\circ}C$)	175	150
5	Operating junction temperature, ($^{\circ}C$)	150	150
6	R_{thja} ($^{\circ}C$/W)	0.1	0.27
	Z_{thja} (for 10 ms)	0.04	0.24
	Z_{thja} (for 1 ms)	0.018	0.05
7	I_{ds}	400 A, T_c=90 ($^{\circ}C$) 600 A, T_c=125 ($^{\circ}C$)	90
8	Pulse current at case temperature of 25 ($^{\circ}C$)	NA for 1 ms	250 A
9	Weight (g)	140	8
10	Dimension in (mm^3)	110*62*26	TO-247-3 (21*16*5)
11	Cost per device in £	1100	50

The current rating of the CREE module (CAS325M12HM2) is almost five times higher than that of the discrete MOSFET (C2M0025120D). Therefore, a 100 A SSPC is designed with a single CAS325M12HM2 device and will be later compared with the SSPC developed with five C2M0025120D devices in parallel. The positive thermal coefficient of SiC MOSFET devices ensures that parallel-connected devices are free of the thermal runaway [18]. On the other side, those five devices are placed on one heatsink allowing the heat sharing, which tends to force devices balancing the temperature as a hot device heats its neighbours. The topologies are illustrated in Fig. 3 and the selected MOSFETs are shown in Fig. 4. The SSPC built with a single module of CAS325M12HM2 is named as SSPC-S and the SSPC designed with paralleled C2M0025120D devices named as SSPC-M in this paper.

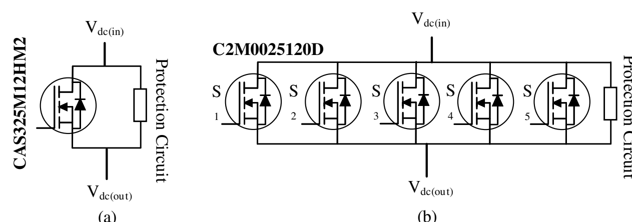

FIGURE 3: Two different design of the SSPC for 100 A rating a. Single module of CAS325M12HM2 (SSPC-S) b. Five discrete MOSFETs (C2M0025120D) in parallel (SSPC-M).

FIGURE 4: Two different MOSFETs selected for the design of SSPCs.

III. THERMAL ANALYSIS OF THE SSPCS

A. JUNCTION TEMPERATURE ESTIMATION OF THE MOSFETS

A heat dissipation path of any semiconductor device consists of the thermal impedance of the MOSFET (R_{thja}). This R_{thja} includes thermal impedance from the junction to the case R_{thjc} (which depends on its junction/case area), the device case to the heat sink assembly R_{thcs} and the heatsink to the ambient R_{thsa}. The approximate thermal impedance circuit from the junction of the device to ambient is illustrated in Fig. 5 [19].

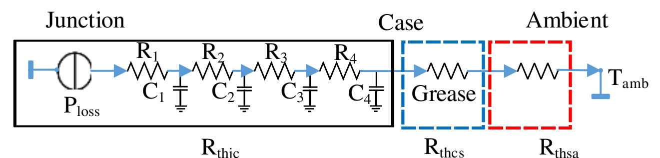

FIGURE 5: The equivalent thermal circuit of SSPCs.

The physical current limit of the MOSFETs is influenced by the size/shape/material of the heat sink and intrinsic thermal resistance of the device itself. Therefore, the actual power dissipating and current carry capacity of the MOSFETs depend on the heat dissipating path of the MOSFET-heat sink assembly. The nominal power dissipation (P_{loss}) and nominal drain current ($I_{d(mos)}$) of the MOSFETs can be approximated by (1) and (2) [15], [20], [21]:

$$P_{loss} = \frac{T_j - T_a}{R_{thja}} \tag{1}$$

$$I_{d(mos)} = \sqrt{\frac{T_j - T_a}{R_{thja} R_{dson(max)}}} \tag{2}$$

where, T_j and T_a are the operating junction temperature and the ambient temperature of the MOSFETs, respectively. The parameters, $R_{dson(max)}$ and R_{thja} are the maximum on-state resistance of the MOSFET and thermal resistance from junction to ambient, respectively.

The continuous conduction loss of the SSPC will have an impact on the MOSFET junction temperature. The actual junction temperature ($T_{j(act)}$) of the MOSFET during nominal operation of the SSPC can be theoretically calculated as [15], [20]:

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$$T_{j(act)} >= \frac{I_{dc}^2}{n^2} R_{dson(max)} R_{thja} + T_a < T_{j(max)} \quad (3)$$

where, n is the number of MOSFETs in parallel, I_{dc} is the nominal current rating of the SSPC. This junction temperature should be less than $T_{j(max)}$, the maximum allowed junction temperature.

During the transient scenarios, a peak transient current ($I_{d(mos)peak}$) should be considered for the SSPC thermal design due to the reactive devices in the system. It is normally higher than the nominal current rating. The peak power dissipation (P_{max}) and the physical limit of the peak current ($I_{d(mos)peak}$) of the MOSFET can be expressed as (4) and (5) [15], [20], [21]:

$$P_{max} = \frac{T_j - T_c}{Z_{thja}} \quad (4)$$

$$I_{d(mos)peak} = \sqrt{\frac{T_j - T_c}{Z_{thja} R_{dson(max)}}} \quad (5)$$

where Z_{thja} is the transient thermal impedance of the device.

MOSFET devices within the SSPC are exposed to a various over-current scenario. The actual junction temperature ($T_{j(act)}$) of the device during those scenario depends on the magnitude of overload current (I_p) and transient thermal impedance (Z_{thja}) of the MOSFET and can be evaluated employing (6) [15], [20].

$$T_{j(act)} >= \frac{I_p^2}{n^2} R_{dson(max)} Z_{thja} + T_c < T_{j(max)} \quad (6)$$

The junction temperature of the devices during nominal and over-current scenarios should be within the specified limit (6) in order to prevent the thermal breakdown of semiconductor devices.

B. THERMAL SIMULATION OF THE SSPCS

Conduction loss is the major loss of SSPCs during nominal operation. Switching loss of SSPCs can be neglected when calculating their nominal efficiencies. During a steady state, the anti-parallel diode never conducts and therefore do not contribute to any loss of the SSPC. Thus, for an SSPC with n MOSFET devices in parallel, the conduction loss ($C_{l(mos(sspc))}$) and efficiency ($\eta_{mos(sspc)}$) of the SSPC can be estimated as:

$$C_{l(mos(sspc))} = \frac{I_{dc}^2}{n} R_{dson(T_j(act))} \quad (7)$$

$$\eta_{mos(sspc)} = \left(1 - \frac{I_{dc}}{nV_{dc}} R_{dson(T_j(act))}\right) \quad (8)$$

where $R_{dson(T_j(act))}$ is the on-state resistance at an actual junction temperature $T_{j(act)}$ and V_{dc} is the voltage across on the SSPC.

With (2) – (6), the number of devices for paralleling can be defined using the datasheets of CAS325M12HM2 and C2M0025120D. The efficiency of one SSPC can be derived using (7) and (8). The ambient temperature is assumed to be $85°C$ which is a nominal temperature within the aircraft power electronics bay. As shown in Table II, with the device CAS325M12HM2 (SSPC-S), there is no need for device paralleling to fulfil (3) and (6). With the discrete device C2M0025120D (SSPC-M), the number of devices required in parallel is five to meet the thermal requirement.

The thermal simulations for both the SSPCs are carried out in PLECS software. The module/devices are assumed to be mounted to a heat sink assembly with a thermal resistance of 0.2 $°C$/W. A detailed datasheet of the MOSFETs is also obtained from the supplier and employed for the PLECS thermal studies. The simulation of the SSPC is accomplished to evaluate the steady-state operation as well as over-current scenarios. The SSPC-S suffers from 70 W loss during its nominal operation. This loss increases the junction temperature of the MOSFET module to $105°C$. Once the steady state during nominal operation is achieved, a cascaded over-current situation is applied to the SSPC (125 A for 120s, 150A for 5s, 200A for 10ms and 400A for 1ms). For the SSPC-S, the maximum junction temperature of $146°C$ is observed during the worst-case over-current scenario as presented in Fig. 6.

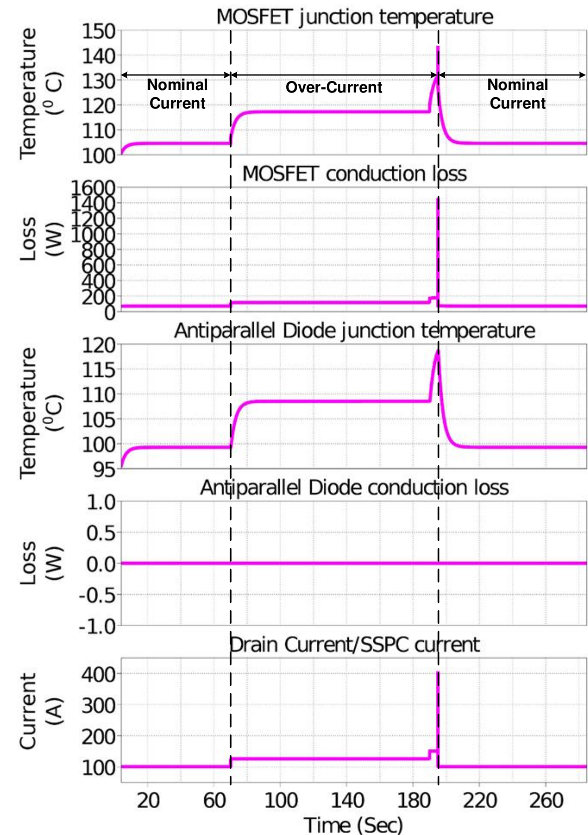

FIGURE 6: Simulation results of the junction temperature and loss of a MOSFET module of the SSPC-S.

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The thermal simulation of SSPC-M with five discrete MOSFETs is shown in Fig. 7. The loss per MOSFET device at steady state is approximately 18 W which amounts the total loss to 90 W. This meant that the SSPC-M has 20 W more losses compared to the SSPC-S. The maximum junction temperature of the discrete device during the worst over-current scenario reaches up to $125°C$. Even though the loss of SSPC-M is higher, both the SSPCs exhibits a similar safety margin of $25°C$ in the maximum junction temperature during the worst scenario. The summary of the thermal simulation for both the SSPCs is listed in Table 2.

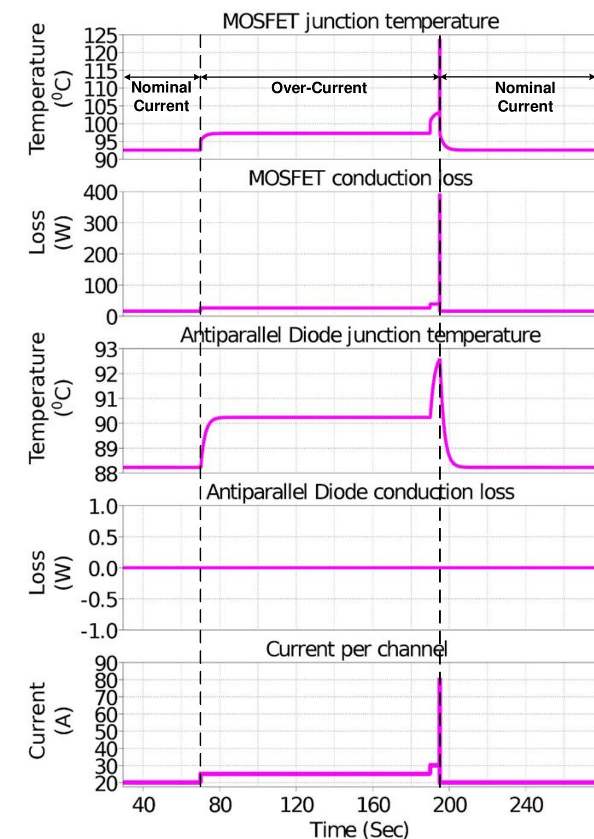

FIGURE 7: Simulation results of the junction temperature and loss per device of a discrete MOSFET device used in the SSPC-M.

IV. TURN-OFF ANALYSIS OF THE SSPCS

In this section, the tripping operation of SSPCs and its impact on the junction temperature are investigated.

A. VOLTAGE STRESS ACROSS SEMICONDUCTORS DURING TRIP-OFF PROCESS

Once the load current through SSPC exceeds the specified i^2t limit, MOSFETs will switch off. The sudden breaking of the current induces voltage spikes across the device. The magnitude of voltage spike depends on transmission line inductances, magnitudes of over current, and the fall-time of

TABLE 2: The semiconductor devices selected for the SSPC design

S.No	Parameters	MOSFET Module CAS325M12HM2	MOSFET C2M0025120D
1	Number of parallel MOSFETs	1	5
2	R_{thca} in $°C$/W	0.2	0.2
3	Max junction temperature during nominal current	105	93
4	Max junction temperature during over current	146	125
5	Conduction loss per device/module during steady state (W)	70	18
6	Total conduction loss of the SSPC (W)	70	90

the current (t_{fall}). The transient voltage stress ($V_{s/w}$) across the semiconductor device during a turn-off process can be evaluated as [17]:

$$V_{s/w} = V_{dc} + L_{dc}\frac{\Delta I_p}{t_{fall}} \tag{9}$$

where L_{dc} is the inductance of DC transmission lines.

Considering the peak current (I_p) of the SSPC is four times of the nominal current during trip-off and this current should be cut off in the range of μs, the peak voltage across the MOSFET could be more than 1200 V in the studied SSPC. The LTSPICE simulation during turn-off operations (without any protection circuit) for SSPC-S built with a single high current module is shown in Fig. 8. As can be seen, the voltage spike across the device reaches over 1.4 kV when the SSPC is tripped from 400 A to 0 A within 10 μs and the peak power dissipated in the device is around 450 kW (energy of 2.3 J). Simulation results of SSPC-M with a seminar scenario is presented in Fig. 9. As can be seen, when a current of each module falls from 80 A (total current 400 A) to 0 A during the tripping operation, a transient voltage up to 1600 V is introduced and a peak power dissipation of 130 kW (energy of 0.065 J) occurs for each device. If the SSPCs are operated without any protection circuit, the energy during the trip-off process would be dissipated across the junction of the MOSFET and the semiconductor device might be damaged.

B. ENERGY DISSIPATED BY TRANSIENT VOLTAGE SUPPRESSION CIRCUITS

The induced high transient voltage across the MOSFET needs to be clamped and the associated energy needs to be dissipated somewhere other than semiconductors. A paralleling circuit, referred to as a transient voltage suppression (TVS) circuit, is used to protect semiconductor switching devices within SSPCs. This TVS device eventually prevents the semiconductor device from over-voltage stress and transient overheating of the device junction.

The TVS device works in two modes: a) normal mode and b) protection mode. During normal operations, the TVS acts as an open circuit path and nearly no current flows

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through it. However, when the SSPC trips, the current will be bypassed via parallel TVS device. The stored energy in the line inductance is dissipated through the TVS and the voltage across the MOSFET device is clamped to a designed voltage level across the TVS device [22].

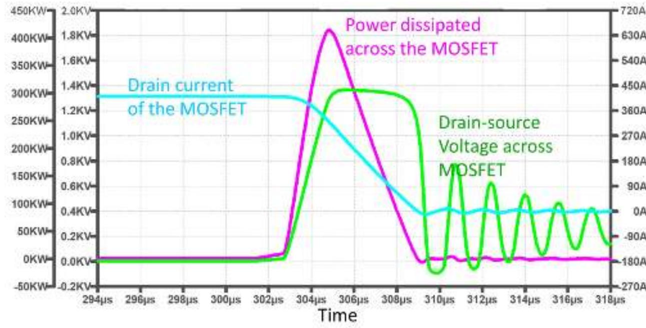

FIGURE 8: The current, voltage, and power dissipated across the MOSFET of SSPC-S without any protection.

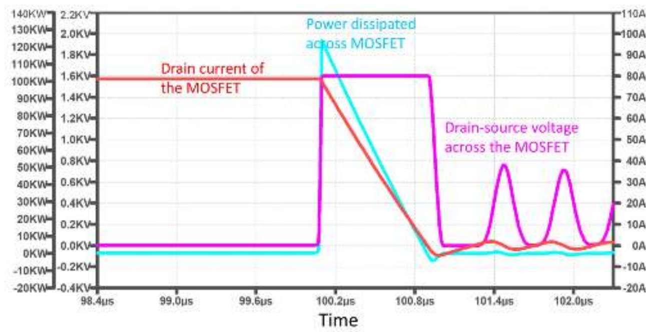

FIGURE 9: The current, voltage, and power dissipated across the discrete MOSFET (C2M0025120D) without any protection.

The inductive energy stored (W_l) in a transmission line associated inductor can be expressed in (10). As can be seen, the amount of energy stored in the line inductor is greatly influenced by the magnitude of breaking current. In our study cases, this current can be four-nine times higher than the nominal current.

$$W_l = \frac{1}{2} L_{dc} I_p^2 \tag{10}$$

During the tripping operation of the SSPC, the extra energy is injected into the circuit before the voltage across the MOSFET reaches the clamping voltage (V_{CB}). This injected energy (W_{source}) can be evaluated as [22]:

$$W_{source} = \frac{L_{dc} V_{dc} I_p^2}{2(V_{CB} + V_{dc})} \tag{11}$$

The total energy (W_{total}) that needs to be dissipated across the TVS device during the complete turn-off operation of the SSPC can be calculated as (12) [22]. The energy that needs to be dissipated across the SSPC is calculated around 2 joules.

$$\begin{aligned} W_{total} &= \frac{1}{2} L_{dc} I_p^2 + \frac{L_{dc} V_{dc} I_p^2}{2(V_{CB} + V_{dc})} \\ &= \frac{1}{2} L_{dc} I_p^2 \left(1 + \frac{V_{dc}}{(V_{CB} + V_{dc})}\right) \end{aligned} \tag{12}$$

C. SELECTION OF TVS CIRCUIT

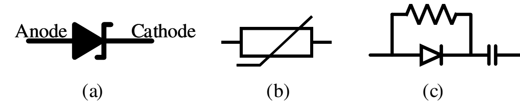

FIGURE 10: Transit voltage suppression devices a) Zener diode; b) Metal oxide varistor; c) RCD (resistor-capacitor-diode) snubber.

The TVS devices can be broadly categorized into p-n junction based device, varistor based device, and conventional snubber circuit, as shown in Fig.10. The p-n junction based Zener/Avalanche/TVS diode functions in the same way. When the SSPC is operating during nominal operation, only the leakage current flows through these devices. But during the tripping operation, the p-n junction of these devices breaks down at the clamping voltage and the overload current (for few ms) is bypassed through these devices. The inductive energy is dissipated in the p-n junction of these devices. The TVS diode is mostly used in switch-mode power supplies. However, the energy dissipation requirement of the SSPCs is very high and therefore, multiple TVS diodes need to be connected in parallel for TVS operation. In addition, the cost of the TVS diode is higher than other protection devices. The comprehensive comparison of various protection mechanisms has been presented in [17].

A metal oxide varistor (MOV) is a voltage-dependent resistor which offers higher voltage and surges current ratings than that of p-n junction based TVS devices. A MOV consists of a large number of micro-varistors that are made up of uniformly distributed zinc oxide and other metallic oxide crystals. The MOVs are suitable for non-repetitive surge protection which requires high energy dissipation. The detailed study of the various protection circuits is explained in our previous study [17]. The conclusion in [17] is that either TVS diode or MOV can be used without snubber circuit as transient voltage suppression device. However, the cost and energy handling capacity of the MOV is better than that of TVS diode. In addition, the internal thermal protection of the thermally protected MOV provides fail-safe operation during the thermal breakdown. Therefore, the MOV is selected for transient voltage suppression.

SSPCs are not continuously switching device like inverters or rectifiers and the magnitude of inductive energy stored in the line inductance of the SSPC is higher than any switch mode power supply (SMPS). Therefore, the primary protection of the SSPC is carried out using a thermally protected

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MOV (TMOV-TMOV20RP275M) parallel to the MOSFETs. The clamping voltage of the selected MOV is around 700-800 V. Once the voltage across the SSPC exceeds the clamping voltage, the peak current of the SSPC is bypassed through the MOV and the tripping energy associated with the circuit is dissipated across its junction. The switching characteristics of the SSPC-S and SSPC-M with MOV protection are shown in Fig. 11 and 12, respectively. The use of MOV has reduced the duration of over-current flowing through the MOSFET and the power dissipated across its junction.

Tripping operation of the SSPC has a substantial thermal impact on the junction temperature of the semiconductor device. The increase in junction temperature depends on the peak power during switching and the transient thermal resistance of the device. The increase in the junction temperature ($\Delta T_{j(act)}$) of the device can be approximated as:

$$\Delta T_{j(act)} \approx \frac{1}{2} I_p V_{CB} Z_{thja(t)} \tag{13}$$

The junction temperature increment of the MOSFET module is reduced to 31 $^{\circ}C$ from 66 $^{\circ}C$ for single module SSPC-S. There has been a significant decrement in the junction temperature of discrete MOSFET for the SSPC-M too. The MOV truncated the energy dissipated across the p-n junction of the MOSFET from 0.08 J to 4.2*10^{-3} J with increment in junction temperature reduced to 32 $^{\circ}C$.

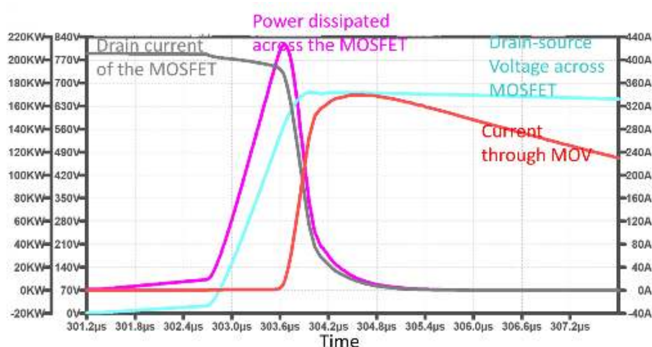

FIGURE 11: The current, voltage, and power dissipated across MOSFET module for SSPC-S with MOV protection.

D. SNUBBER CIRCUITS FOR INDIVIDUAL MOSFET DEVICES

The energy dissipated across the junction of the MOSFETs can be further reduced using soft-switching strategy. This can be carried out by employing individual turn-off snubber across the MOSFETs. The snubber circuit reacts first before the MOV goes into the protection mode, which further reduces the energy dissipating in the junction of the MOSFETs. The traditional turn-off snubber capacitor can be designed for the protection of the SSPC. The value of the clamping capacitor (C_{clamp}) can be approximated as:

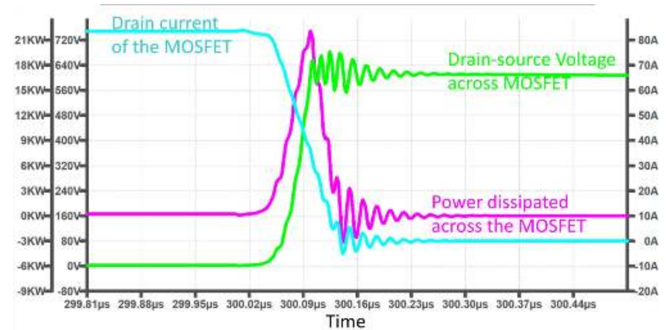

FIGURE 12: The current, voltage, and power dissipated across the discrete MOSFET (C2M0025120D) of SSPC-M with MOV protection.

$$C_{clamp} \approx \frac{2W_{total}}{(V_{CB})^2} \approx \frac{2L_{dc}I_p^2}{(V_{CB})^2}\left(1 + \frac{V_{dc}}{(V_{CB}+V_{dc})}\right) \tag{14}$$

The clamping voltage can be set 850 V for 1200 V MOSFET device. The value of the snubber capacitor can range from 30 to 60 μF. The size of the snubber capacitor for this large capacitance would be large for 1200 V rating and therefore reducing the power density of the SSPC. Moreover, the high value of the capacitance causes inrush current during the turn-on operation which may induce false tripping of the SSPC. Therefore, capacitive snubber without MOV is not advised to employ for the protection of the SSPCs.

The SSPC can be protected by RCD snubber. However, this configuration increases the component counts of the SSPC. The value of snubber capacitor (C_{snub}), snubber resistance (R_{snub}), and power dissipated in the snubber resistor (P_{snub}) in snubber circuit can be evaluated as [23], [24]:

$$C_{snub} \approx \frac{L_{dc}I_p^2}{(V_{CB}-V_{dc})^2} \tag{15}$$

$$R_{snub} \approx \frac{1}{6C_{snub}f_{sw}} \tag{16}$$

$$P_{snub} \approx \frac{C_{snub}(V_{CB}-V_{dc})^2 f_{sw}}{2t_{tripping}} \tag{17}$$

where $t_{tripping}$ is the tripping time of the SSPC.

The capacitance value of the RCD snubber is around 20-30 μF. Moreover, the selection of snubber diodes needs to be carried out based on the peak current rating of the SSPC. The peak current rating of the diode should be higher than four times nominal current of the SSPC. In order to meet the peak current requirement, the diode with high current rating like GP2D060A120B (from Global Power Technologies Group) are required for snubber design. The use of RCD snubber for bidirectional SSPC may adds up three to six additional components in the SSPC.

Since SSPCs are not continuous switching devices, the power loss associated with the snubber circuit during

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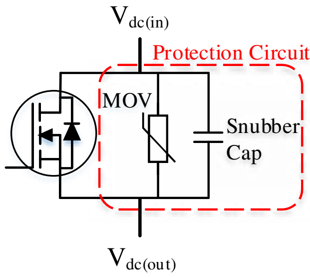

FIGURE 13: The protection circuit of the SSPC with MOV and snubber capacitor.

the nominal operation can be ignored. For the protection of the SSPC during tripping, the soft-switch assisting capacitor/capacitor-resistor without diode along with energy dissipating MOV is employed across the MOSFET very close to the drain and source as shown in Fig. 13. These capacitors assist the soft-switching turn-off operation of the MOSFET and the MOV acts as the main voltage clamping and energy dissipating device. The value of the snubber capacitor for soft turn-off can be evaluated as:

$$C_{snub} \approx \frac{I_p \Delta t}{V_{CB}} \tag{18}$$

where Δt is the rise time of the voltage across the SSPC.

The value of the snubber capacitor for SSPC-S is calculated around 0.7 μF. The tripping operation of the SSPC-S with MOV and snubber capacitor is shown in Fig. 14. The peak power dissipation across the MOSFET module is reduced to 45 kW and eventually minimized the increase in junction temperature to 6 $°C$.

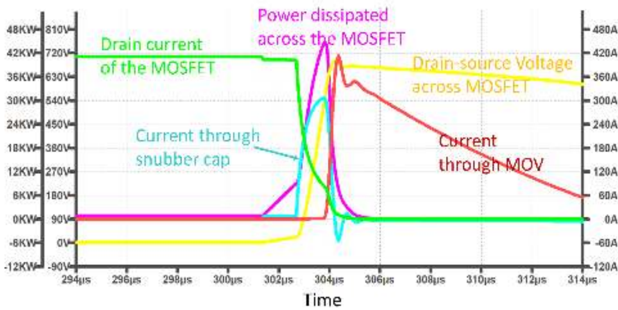

FIGURE 14: The current, voltage, and power dissipated across the MOSFET module of SSPC-S during turn-off with a MOV and capacitive snubber.

The use of snubber capacitor induces surging current during turn-on operation of the SSPC. The magnitude of the inrush current is a function of snubber capacitance and current rise time as expressed in 19. The inrush current of the SSPC-S with the snubber capacitor is illustrated in Fig. 15. The value of peak inrush current is around 200 A for 2 μs duration. The increase in junction temperature due to inrush current is approximately 5-6 $°C$.

$$I_{inrush} = \frac{C_{snub} V_{dc}}{\Delta t} \tag{19}$$

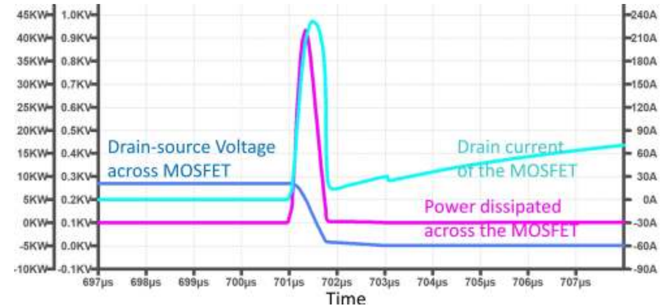

FIGURE 15: The current, voltage, and power dissipated across the MOSFET of SSPC-S during turn-on operation

For the SSPC-M, the soft-switching capacitor with capacitance 0.01 μF is connected across each discrete MOSFET. The peak power dissipation across the switch has been drastically reduced to 2.7 kW with an increase in junction temperature about 6 $°C$. The soft turn-off operation of the SSPC-M with MOV and snubber capacitor is illustrated in Fig. 16.

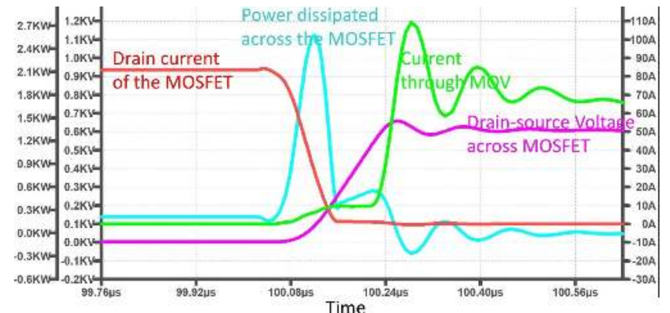

FIGURE 16: The current, voltage, and power dissipated across the MOSFET of SSPC-M during turn-off with a MOV and capacitive snubber.

The use of capacitive snubber increases the peak power dissipation during turn-on. The turn-on operation of the SSPC-M with snubber capacitor and MOV is presented in Fig. 17. The peak power dissipation is around 8 kW with an approximate increase in junction temperature by 10-12 $°C$. The increase in turn-on loss across the switch and high inrush current can be reduced by replacing C snubber with RC snubber. The value of snubber resistance required can be calculated using (16).

The summary of the LTSPICE simulation with and without the protection circuit is presented in Table 3. The simulation results advise using MOV and a small snubber cap for the protection of the SSPC. This protection mechanism will be validated experimentally in the next section.

V. EXPERIMENTAL RESULTS OF THE SSPCS

The SSPCs are built for the validation of the thermal and transient simulation carried out in the earlier sections. The

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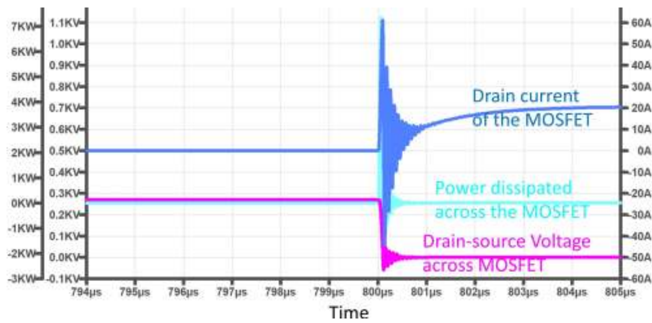

FIGURE 17: The current, voltage, and the power dissipated across the MOSFET of SSPC-M during turn-on operation.

TABLE 3: Power/Energy dissipated in the junction of the MOSFET and increase in junction temperature of the device employed in SSPC design

	Peak Power per MOSFET (kW)	Energy dissipated across the MOSFET (J)	Transient thermal resistance for 10 μs	Increase in junction temperature ($^{\circ}C$)
SSPC-S (no protection)	440	3.52	3.00e-04	66
SSPC-S (with MOV)	210	0.42	3.00e-04	31
SSPC-S (MOV+Cap)	46	0.092	3.00e-04	7
SSPC-M (no protection)	130	0.08	3.00e-03	195
SSPC-M (with MOV)	21	4.2x10e-3	3.00e-03	32
SSPC-M (MOV+Cap)	2.4	5.4x10e-4	3.00e-03	4

thermal performances of the SSPCs are accessed at a nominal current of 100 A. The tripping operation is carried out at 1.5 times the nominal current. The impact of protection during tripping is also included in this section.

The experimental prototype of the SSPC-S is shown in Fig. 18. The hardware consists of voltage supply source (which converts 28 V into 15 V), semiconductor module (CAS325M12HM2), a heat sink (P135-100-35), a driver, and protection circuits. The protection circuits include the individual semiconductor protection with snubber capacitors (0.7 μF) located very close to drain-source of the device and single TMOV (TMOV20RP250M) is employed for dissipating the tripping energy.

The prototype of the SSPC-M consists of five discrete devices (C2M0025120D) with the individual driver mounted in the same sized sink as compared with SSPC-S. Each MOSFET is protected with snubber capacitor (0.01 μF) and a common TMOV (TMOV20RP250M) for the SSPC protection. The hardware prototype for the laboratory testing of the SSPC-M is presented in Fig. 19.

The simulations of both the SSPCs are carried out at 85 $^{\circ}C$. However, the laboratory experiment is conducted at room temperature (25 $^{\circ}C$). The DC source is created by the parallel connection of two 15 kW bi-directional power

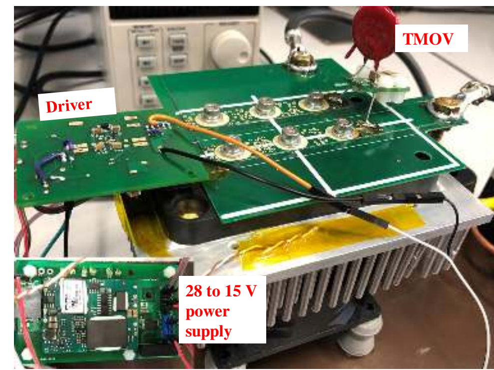

FIGURE 18: The laboratory prototype of the SSPC-S.

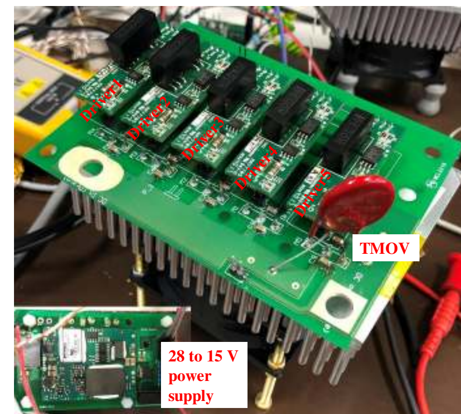

FIGURE 19: The laboratory prototype of the SSPC-M.

supplies (SM500-CP-90). The maximum current of the DC sources is limited up to 180 A. The steady-state continuous operation of the SSPCs is carried out at rated current of 100 A. The thermal status of the SSPC-S after a continuous operation is shown in Fig. 20. The heat-sink temperature of SSPC-S raises to 40 $^{\circ}C$ from 25 $^{\circ}C$. However, the PCB temperature is slightly higher and got settled at 46 $^{\circ}C$. The voltage drop across the SSPC-S is 0.4 V and the total power loss across the module is 40 W.

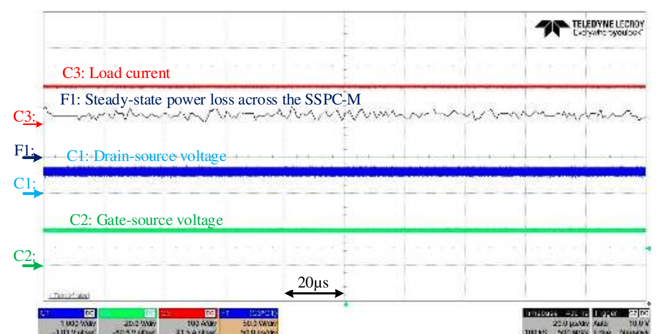

FIGURE 20: The steady state experimental result of the SSPC-S.

The maximum temperature of the heat-sink for SSPC-M reached up to 45 $^{\circ}C$ during nominal operation. However, the maximum PCB temperature notched up to 75 $^{\circ}C$ due to the

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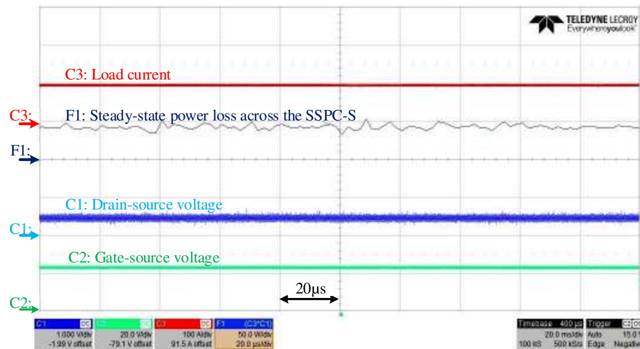

FIGURE 21: The steady state experimental result of the SSPC-M

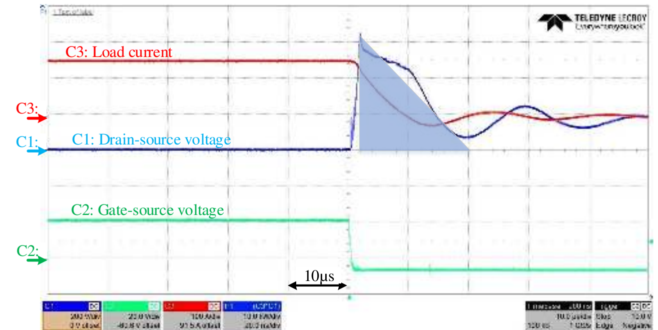

FIGURE 23: The turn-off process of the SSPC-S with additional 20 μH line inductor.

small current channel in the PCB for each MOSFET. The thermal camera is employed to measure the case temperature of the MOSFET device. The maximum case temperature of the discrete MOSFET notched up to 107 $^{\circ}C$. The electrical insulation and thermal paste between the case of the device and heat-sink increased the thermal resistance of the heat-sink assembly. The case temperature can be reduced with better case-to-sink paste and insulation. The voltage drop across the SSPC is around 0.6 V with the total loss around 60 W as shown in Fig. 21. The voltage drop and the total loss across the SSPC are less in the experiments than that of the simulation is due to low ambient temperature during the experiment. The thermal images of the SSPCs after 30 minutes of operation are presented in Fig. 22.

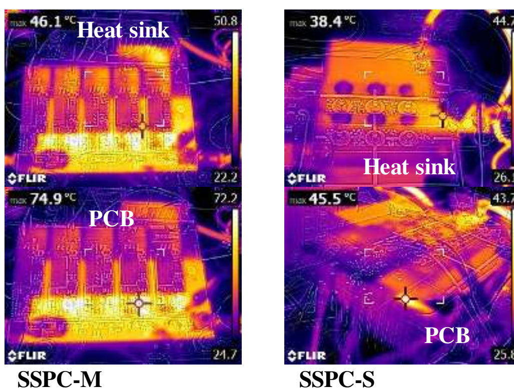

FIGURE 22: The thermal images of the SSPCs during steady-state operation with 100 A current.

The turn-off operation is carried out at 1.5 times of the nominal current (due to the limitation of the power supply) with extra 15 μH line inductance. The total loop inductance of the SSPC-S (MOSFET D-S adding PCB) is around 6 nH, which is lot less than the value of the extra line inductance and therefore has no significant impact of the tripping operation of the SSPC. The tripping operation of modular SSPC is presented in Fig. 23. The peak voltage of across the MOSFET-module is clipped to 650 V and the peak power dissipation across the SSPC is around 48 kW (energy of 0.24 J).

The MOSFETs of the SSPC-M are protected by individual snubber capacitors and a TMOV. The complete turn-off procedure of the SSPC-M is completed within 10 μs with 75 kW peak power dissipated across the SSPC. The use of TMOV has reduced the voltage stress up to 1000 V during tripping operation as shown in Fig. 24. The turn-off operation of the SSPC-M is similar to SSPC-S. However, SSPC-M is more prone to interference and noise as compared with the SSPC-S.

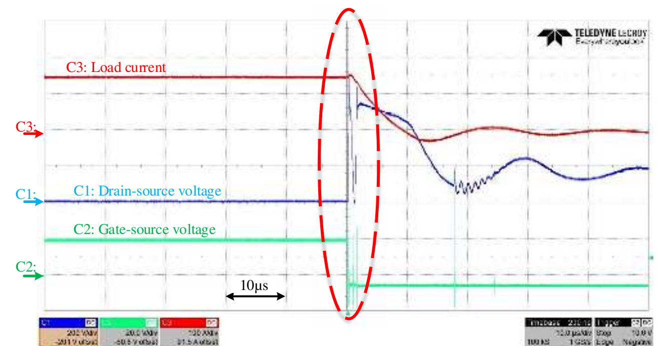

FIGURE 24: The turn-off process of the SSPC-M with additional 15 μH line inductor.

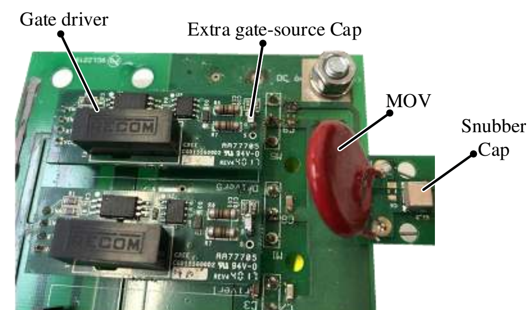

FIGURE 25: Gate drivers with extra gate-source capacitance and snubber capacitor.

The gate-source voltage suffers from ringing problem during turn-off of the SSPC-M, which leads to voltage overshoot in the drain-source voltage across the MOSFETs. This overshoot cannot be mitigated with the use of MOV due to slow

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response time of the MOV as compared with the duration of over-voltage. Therefore, the gate drivers for the MOSFETs are modified with extra gate-source capacitance (10 nF) and an extra snubber capacitor of (0.2 μF) is added parallel to the MOV, as shown in Fig. 25. The turn-off response of the SSPC-M with the modified circuit is presented in Fig. 26. The voltage overshoot and total power dissipated across the SSPC is reduced to 600 V and 45 kW (energy of 0.22 J), respectively.

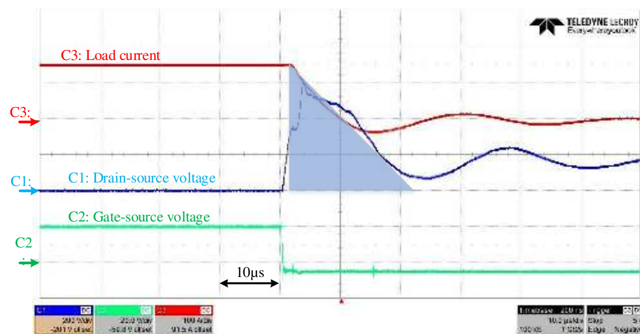

FIGURE 26: The turn-off process of the SSPC-M with additional 15 μH line inductor with extra snubber capacitance (0.2 μF) and gate-source capacitance for each driver (10 nF).

VI. POWER DENSITY AND COST ESTIMATION OF THE SSPC

The HVDC bipolar architecture of an aerospace electrical system consists of two power lines for the positive and negative bus. The SSPCs are placed for both the power lines as shown in Fig. 27. The various approximated parameters of the SSPC-M and SSPC-S are listed in Table 4. The SSPC-M and SSPC-S have comparable power density. However, the estimated cost of SSPC-M is a lot less than the cost of SSPC-S. This is due to the very high price of CREE MOS module employed in the design of SSPC-S. However, the use of multiple TO-247 devices in parallel increases the difficulty for thermal management and adds complexity in the design of the PCB. Each MOSFET device comes with individual driver and protection circuit which increases the overall components counts of SSPC-M over SSPC-S and therefore compromising the reliability of the SSPC. Therefore, SSPC-S seems to be a reasonable choice for the design of high current circuit breaker for more electric air-craft.

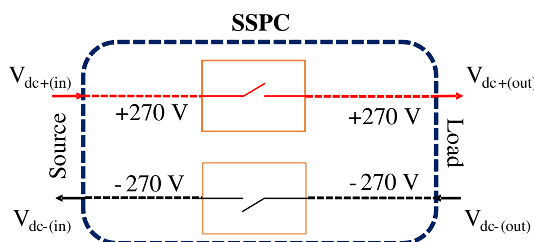

FIGURE 27: The schematic of the aircraft's bipolar electrical architecture with the SSPCs.

TABLE 4: Comparative evaluation of the SSPC based on the approximated parameters

S.No	Parameters	CAS325M12HM2 based SSPC	C2M0025120D based SSPC
1	Device count	2	10
2	Weight (kgs)	1.6	1.8
3	Power density (kW/kg)	33	30
4	Component Cost (£)	2600	800
5	Component Cost density (kW/£)	20.7	67.5
6	Max Loss (W)	140	180
7	Max Voltage drop (V)	0.7	1
8	Approximate Dimension (mm*mm*mm)	135*200*70	135*200*70

VII. CONCLUSIONS

Two different design approaches for the development of high current SSPC has been presented in this paper. The modular approach consisted of a single high current CREE MOSFET with a simple design and fewer components. However, the cost of the modular SSPC design is higher than the cost of the SSPC built with multiple discrete devices. The SSPC designed with discrete devices was comparable in terms of weight and power density as compared with the other one but suffers from higher voltage drop and steady-state power loss. The steady-state power loss and thermal impact due to conduction loss of both the SSPCs were analysed and later verified in both simulation and hardware environment. The SSPC-S suffered 0.7 V (in simulation) and 0.4 V (in experiment) drops across its terminal with nominal power loss of 70 W (in simulation) and 40 W (in experiment). On the other hand, SSPC-M had voltage drops of 1 V (in simulation) and 0.6 V (in experiment) with heat dissipation of 90 W (in simulation) and 60 W (in experiment). The turn-off operation of both the SSPCs were experimentally validated as well. A protection circuit comprising of a MOV and a snubber capacitor was proposed and adopted for both SSPC-S and SSPC-M. This over-voltage protection circuit clamped the voltage stress to 600-650 V across both the SSPCs. In addition, both the SSPCs were tripped within 10 μs with the total dissipated energy of around 0.2-0.25 J at breaking current of 150 A.

The SSPC-S seems to have higher efficiency, fewer devices (more reliable), and comparable power density than that of the SSPC-M. Therefore, SSPC designed with high current MOSFET modules can be considered as the replacement of ECBs for future aircraft.

REFERENCES

[1] J. Chen, C. Wang, and J. Chen, "Investigation on the selection of electric power system architecture for future more electric aircraft," *IEEE Transactions on Transportation Electrification*, vol. PP, no. 99, pp. 1–1, 2018.
[2] A. Barzkar and M. Ghassemi, "Electric power systems in more and all electric aircraft: A review," *IEEE Access*, 2020.
[3] J. K. Nøland, M. Leandro, J. A. Suul, and M. Molinas, "High-power machines and starter-generator topologies for more electric aircraft: A technology outlook," *IEEE Access*, vol. 8, pp. 130 104–130 123, 2020.
[4] S. Kim, G. Ulissi, S.-N. Kim, and D. Dujic, "Protection coordination for reliable marine dc power distribution networks," *IEEE Access*, vol. 8, pp. 222 813–222 823, 2020.
[5] Z. Miao, G. Sabui, A. M. Roshandeh, and Z. J. Shen, "Design and analysis of dc solid-state circuit breakers using sic jfets," *IEEE Journal of Emerging*

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and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 863–873, Sept 2016.

[6] L. L. Qi, A. Antoniazzi, L. Raciti, and D. Leoni, "Design of solid-state circuit breaker-based protection for dc shipboard power systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 260–268, March 2017.

[7] X. Song, C. Peng, and A. Q. Huang, "A medium-voltage hybrid dc circuit breaker, part i: Solid-state main breaker based on 15 kv sic emitter turn-off thyristor," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 278–288, March 2017.

[8] C. Peng, X. Song, A. Q. Huang, and I. Husain, "A medium-voltage hybrid dc circuit breaker—part ii: Ultrafast mechanical switch," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 289–296, March 2017.

[9] L. L. Qi, A. Antoniazzi, L. Raciti, and D. Leoni, "Design of solid-state circuit breaker-based protection for dc shipboard power systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 260–268, March 2017.

[10] W. Chen, H. Tao, C. Liu, Y. Xia, Y. Shi, Y. Liu, C. Liu, J. Liu, Q. Zhou, Z. Li, and B. Zhang, "Evaluation of cs-mct in dc solid-state circuit breaker applications," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 5465–5473, Sep. 2018.

[11] C. Meyer, S. Schroder, and R. W. De Doncker, "Solid-state circuit breakers and current limiters for medium-voltage systems having distributed power systems," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1333–1340, Sep. 2004.

[12] Y. Du, J. Deng, H. Lin, H. Zheng, K. Xiang, and Y. Shen, "Research and experiment of a current-limiting hvdc circuit breaker," *The Journal of Engineering*, vol. 2019, no. 16, pp. 2002–2006, 2019.

[13] X. Liao, H. Li, R. Yao, Z. Huang, and K. Wang, "Voltage overshoot suppression for sic mosfet-based dc solid-state circuit breaker," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 4, pp. 649–660, April 2019.

[14] F. Liu, W. Liu, X. Zha, H. Yang, and K. Feng, "Solid-state circuit breaker snubber design for transient overvoltage suppression at bus fault interruption in low-voltage dc microgrid," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 3007–3021, April 2017.

[15] J. Adhikari, T. Yang, J. Zhang, M. Rashed, S. Bozhko, and P. Wheeler, "Thermal analysis of high power high voltage dc solid state power controller (sspc) for next generation civil tilt rotor-craft," in *2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles International Transportation Electrification Conference (ESARS-ITEC)*, Nov 2018, pp. 1–6.

[16] J. Magnusson, R. Saers, L. Liljestrand, and G. Engdahl, "Separation of the energy absorption and overvoltage protection in solid-state breakers by the use of parallel varistors," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 2715–2722, June 2014.

[17] J. Adhikari, T. Yang, M. Rashed, S. Bozhko, J. Zhang, and P. W. Wheeler, "Transient stability analysis of dc solid state power controller (sspc) for more electric aircraft," in *Aerospace Systems and Technology Conference*. SAE International, oct 2018. [Online]. Available: https://doi.org/10.4271/2018-01-1927

[18] B. Yu, L. Wang, and D. Ahmed, "Drain–source voltage clamp circuit for online accurate on-state resistance measurement of sic mosfets in dc solid-state power controller," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 331–342, 2019.

[19] K. Ma, N. He, M. Liserre, and F. Blaabjerg, "Frequency-domain thermal modeling and characterization of power semiconductor devices," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7183–7193, Oct 2016.

[20] D. A. Molligoda, P. Chatterjee, C. J. Gajanayake, A. K. Gupta, and K. J. Tseng, "Review of design and challenges of dc sspc in more electric aircraft," in *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, Dec 2016, pp. 1–5.

[21] A. . O. S. Anup Bhalla, "Thermal resistance characterization of power mosfets," in *Alpha and Omega Semiconductor, January 2003*.

[22] E. d. Norum, "Design and operation principles of dc circuit breakers - development of a solid state dc breaker for the ntnu/sintef smart grid and renewable energy laboratory," Ph.D. dissertation, NTNU, 2016.

[23] R. C. Yi Zhang, Saed Sobhani, "Snubber considerations for igbt applications," in *International Rectifier Applications Engineering*.

[24] Y. Yamashita, J. Furuta, S. Inamori, and K. Kobayashi, "Design of rcd snubber considering wiring inductance for mhz-switching of sic-mosfet," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2017, pp. 1–6.

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